On the failure of graphene devices by Joule heating under current stressing conditions

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The behaviour of single layer graphene sections under current-stressing conditions is presented. Graphene devices are stressed to the point of failure and it is seen that they exhibit Joule heating. Using a simple 1-D model for heat generation, we demonstrate how to extract values for the resistivity and thermal coefficient of resistance of graphene devices from their current-voltage characteristics. We also show that graphene flakes with a large number of ripples and folds have higher resistance and fail along a connected pathway of folds.

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Graphene is being touted as the wonder material of the 21st century due to its impressive electrical and mechanical properties [1, 2]. It has been suggested that graphene may replace Cu as the material of choice for interconnects in circuits as (i) it has better electrical and thermal conductivity and (ii) it does not suffer from electromigration [3]. With this application in mind, the electrical properties of graphene segments [4] and graphene nano-ribbons (GNRs) [5] under current-stressing conditions have been reported, with particular interest in their failure modes. Empirical relationships between resistance and breakdown current density have been observed, and it has been shown that GNRs are capable of sustaining current densities up to as large as 2.8 $\times 10^8$ A/cm^2, comparable to Carbon nanotubes (CNTs) [6]. By contrast, metal nanowires with similar dimensions can sustain current densities up to a maximum of 1.8 $\times 10^8$ A/cm^2, dropping to below 1 $\times 10^7$ A/cm^2 for nanowires with widths below 20 nm. This is in stark contrast to the maximum current density that can be sustained by bulk conductors, of order 1 $\times 10^6$ A/cm^2. In the case of metal nanowires, it has been shown that the maximum current density depends strongly on the substrate upon which the nanowires are placed [7], a fact that has not been taken into consideration with graphene devices before. As the dominant mechanism for failure of graphene devices is due to Joule heating, the substrate plays a key role, as it acts as a heat sink. As typical graphene devices are placed on circa. 90-300 nm thick SiO_2, the heat dissipation through the substrate will be minimal, so the dominant pathway for heat dissipation will be through the contacts to the device. At elevated temperatures, radiative conduction will also start to play a role [8]. While metal nanowires tend to fail at around 250^{o}C by a combination of electromigration and thermomechanical stress (due to the differential thermal expansion coefficients of the metal and the substrate) brought on by Joule heating, the C-C bonds in graphene are so strong that electromigration does not occur. Also, as graphene is not anchored to the substrate, and is therefore free to buckle, Joule heating should not have any associated thermomechanical stress. The process then by which graphene and CNTs are seen to "burn" via the passage of an electric current is not fully understood. In this article, we apply a simple 1-D model for heat generation and flow that we have previously developed to describe Joule heating in nanowires [7, 9] to the problem of graphene devices. The equation to solve for the excess temperature, T, due to the passage of current is :

$$\nabla^2 T - m^2 T + \frac{Q}{k} = 0. \qquad (1)$$

Where $m = \sqrt{\frac{k_{sub}}{ktd}}$, Q is the power generated per unit volume, $J^2\rho$; and k, t, k_{sub}, & d are the effective thermal conductivity and thickness of the graphene and the SiO_2 substrate, respectively. As the heat dissipation through the SiO_2 and the underlying Si only occurs on one side of the graphene sheet, the effective thermal conductivity of the substrate is ½ it's actual value, or 0.55 $WK^{-1}m^{-1}$. The thermal conductivity of oxide-supported exfoliated graphene is known to be around 600 $WK^{-1}m^{-1}$ [10]. The solution to equation (1) for the dependence of the temperature on position relative to the wire centre, x, takes on a different form in the graphene and the contacts, and is of the form:

$$T_{wire} = -\frac{Q}{2km^2}e^{-mL}(e^{mx} + e^{-mx}) + \frac{Q}{km^2} \text{ in the graphene}$$

and $$T_{contact} = \frac{Q}{2km^2}e^{-mx}(e^{mL} - e^{-mL}) \text{ in the contacts} \qquad (2)$$

where $2L$ is the length of the graphene between the electrodes, i.e. the electrode spacing. It must be pointed out that this model is making the assumption that the electrodes are (i) acting as infinite heat sinks, but in practice they will not, so the model will provide us with a *lower bound* for the excess temperature as a result of Joule heating, and (ii) that the contacts and the graphene are the same material, which they are not. We expect the error associated with this to be minimal, as both have similar thermal conductivities which are orders of magnitude larger than that of the substrate.

This approach allows us to calculate the expected temperature profile of a current-carrying graphene device, and to predict the I-V characteristics of the device. As long as we know the temperature coeffieicnt of resistance of a device, we can predict how the resistance will change with temperature. The same approach has been successful in describing current flow in metallic nanowires under similar conditions [9], without needing to resort to any fitting parameters. The issue we face here is that the reported temperature coefficient of graphene devices covers a large range and appears to be strongly device-dependent. As a consequence of

this, we use the temperature coefficient of resistance as one of the fitting parameters from a best fit from the I-V characteristics to our model.

Devices were fabricated using mechanically exfoliated flakes of single-layer graphene on 90 nm of thermal SiO_2. An electrode pattern was fabricated on top of the graphene using electron-beam lithography and lift-off. The electrode design consisted of two different configurations: in device 1, there were metal lines 2.2 μm across, separated by a gap of 4.2 μm, and with a thickness of 53 nm (3nm Ti, 50 nm Au), whereas in device 2, the electrodes were 2.5 μm across, separated by 2.5 μm, and with the same thickness as device 1. The electrode pattern fans out and expands to form contact pads than can easily be connected using a probe station. Two different devices were created, each with several different, independent graphene strips, of average width 10 μm. Micrographs of both of these devices are shown in Fig. 1. An SEM image of device 1 is also shown indicating the planarity of the device, despite some damage to the edges of the graphene flake caused by the lift-off process. In Figure 2, we show the current-voltage characteristics of several devices, all of which show Joule heating to varying degrees. Several things to note are that (i) after some initial electrode annealing, all devices show similar behaviour, i.e. an increase in resistance with applied current; (ii) the measurements performed here were all in a 2-terminal configuration, so the contact resistance between the metal electrodes and the graphene will have an effect on the measured resistance. For device 1, the 2-terminal resistance spanned the range 0.143-0.196 kΩ , and for device 2, was larger at 0.5-6.45 kΩ. The contact resistance was measured for both devices using a four-point measurement and was found to be 99.6 Ω for device 1 and 113.7 Ω for device 2. The difference in the electrical properties within the devices is due to the fact that in device 1, the graphene flake is relatively flat with an rms roughness of around 0.6 nm, whereas in device 2, it is highly contorted with a large number of folds, yielding an rms roughness of around 4 nm. This is evident in the AFM images shown in Fig. 3. The phase shift of the oscillating AFM cantilever (which is operating in tapping mode) is several tens of degrees different on graphene than it is on the electrode or the SiO_2 substrate, so in Fig. 3, we display both the topography and phase separately. The topography and phase of device 1 are shown in Fig. 3(a) and (b), respectively, and likewise for device 2 in Fig. 3(c) and (d), respectively. In Fig. 3(d), the folds in the graphene can be seen as a network of bright lines, and the pathway along which the device failed is indicated by an arrow. The folds on the graphene act as local hotspots under the passage of current flow, and they are where the failure

occurs. The failure characteristics of device 2 bear this out, as shown in Fig 2(b), where the total failure of the device is preceded by a series of small, localised failures. Local hot regions fail, and over time, as they join up, the entire device fails. It is also clear that Joule heating is less prevalent in device 1, as shown in Figs. 2(c)-(d). It is worth noting that the failed sections of device 1 display stable tunnelling across the resulting nanogaps (Fig. 2(e)), whereas for device 2, no current could be measured after the final failure. A fit of the data in Fig. 2(e) to the Simmons tunnelling model [11] reveals a gap size of 1.5 nm. It can be seen that in all cases, the resistance increases with increasing power dissipation, demonstrating a positive temperature coefficient for the devices, as has been reported by others [10]. This is contrary to what is observed in suspended graphene [12], and is a consequence of the increased scattering in the coupled graphene/substrate system. This is the point at which our model for heat dissipation can be applied to obtain a better understanding of the physics of Joule heating in such systems. The parameter which is unknown is the temperature coefficient of resistance. As the resistance changes with temperature, which in turn depends on the power dissipated within the device, we need to modify the heat transfer solution accordingly. The power generated per unit volume, Q, and the resistance, R, become

$$Q' = \frac{J^2\rho}{1-\alpha\beta I^2} \quad \text{and} \quad R = R_C + \frac{R_0}{1-\alpha\beta I^2} \qquad [3]$$

where α, β R_C and R_0 are the temperature coefficient of resistance, the proportionality constant between power and temperature, the contact resistance and the resistance at room temperature, respectively. We iteratively calculate the value of β for each device and use ρ, α and R_C as fitting parameters. As an example, in Fig. 4(a), we have plotted the calculated current-voltage characteristic of device 2 (as shown in Fig. 2(a)), where the best fit is obtained for the parameters shown in Table 1. As α depends on geometry and will vary significantly from one device to another, a more meaningful quantity than the temperature coefficient of resistance is the temperature coefficient of resistivity, and this can be compared to other materials for reference. For this device, the temperature coefficient of resistivity is found to be 0.153 $\mu\Omega$ .cm.K^{-1}.

β (deg/mW)	ρ (mW .cm)	α (K^{-1})	R_C (Ohm)
4.6	11.3	5.1	113.7

Table 1. Best-fit parameters for device 2.

For comparison to bulk gold, ρ = 2.4 μΩ .cm, the temperature coefficient of resistivity is 0.0083 μΩ .cm [13], a factor of 19 smaller. Therefore, we would expect there to be a noticeable change in temperature in the devices due to Joule heating. In Figures 4(b) and 4(c), we have plotted the expected temperature distribution in one of the devices as well as the dependence of temperature at the centre of the device on current, respectively. By contrast, the best-fit parameters for device 1 are shown in table 2.

β (deg/mW)	ρ (mW .cm)	α (K^{-1})	R_C (Ohm)
1.5	2.8	1.3	99.6

Table 2. Best-fit parameters for device 1.

From these values, we see that (i) the resistivity of the folded graphene sheet is a factor of 11/2.8 ~3.9 larger than that of the smooth graphene sheet, and (ii) the corresponding temperature coefficient of resistance is larger by the same factor, indicating that the reason for both to be larger is the same. The positive temperature coefficient of resistance is indicative of scattering (the electronic mean-free path and there the resistivity scales as $1/T$), usually with the substrate. As it is larger in the case of the folded graphene, we propose that the folds themselves are responsible for much of the scattering. In line with Mathiessen's rule, thermal conductivity scales with electrical conductivity (this is valid down to below 20 nm in metallic nanowires [14]) so it is reasonable to expect that the thermal conductivity of the graphene is a factor of 3.92 lower in the folded than the flat graphene. Our model shows that this is still so much higher than the thermal conductivity of the substrate that it makes little difference to the heat flux and the temperature. The reason for the increased temperature coefficient of resistance then has to be the increased scattering in the folded graphene. As the fold pattern is spatially varying, we would

expect that the temperature distribution is position-dependent, with local hot-spots coinciding with regions of increased resistance, i.e. the folds. This is consistent with our observations indicating that the failure was along a connected pathway of folds. In all devices, the calculated value of temperature at which failure occurs was within the range 140-160 degrees C. Clearly this is too low for oxidation/burning, but it must be remembered that our calculations show the average peak temperature, rather than the temperature at any local hotspots, which will be significantly higher. As the number of layers of graphene increases, the resistance increases [15], and the ripples can be seen as regions where the single-layer graphene is effectively double or triple-layer. Hence, the resistance of the ripples is larger than the surrounding areas, by up to a factor of 3 [15], which from our model indicates that the local temperature may be in excess of 420 ^{0}C immediately prior to failure. We must bear in mind that our model gives us a lower bound on the temperature, as the electrodes are not large enough to act as infinite heat sinks. It is known that defects start appearing in graphene due to oxidation at temperatures as low as 220 ^{0}C, [16] so we propose that the local heating that occurs along the folds leads to an unzipping of the graphene layer, eventually resulting in failure. By contrast, in device 1 where there are no folds on the graphene, this process occurs at random nucleation sites, and lines of defects are found between the electrodes. This is shown in Fig. 3(c) of a partly-failed section in device 1 where the AFM image reveals two tears stretching in straight lines between the electrodes.

To conclude, we have shown that graphene with a high density of folds has a higher resistance and temperature coefficient of resistance than planar graphene. We have also shown that application of a model for Joule heating allows us to predict the current-voltage characteristics of graphene devices under large current levels. Folded graphene fails in steps by electroburning/unzipping along a connected pathway of folds whereas planar graphene tends to fail in a single step along straight lines stretching between the electrodes.

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FIGURE CAPTIONS

Fig. 1. Optical micrographs of (a)-(d) graphene device 1 showing the monolayer graphene flake (a) before the electrodes were deposited, (b) after the electrodes were deposited, (c) zoom-in of the device region (d) SEM image showing the graphene flake and the electrodes; (e) optical micrograph of graphene device 1 before the electrodes were deposited. No cracks are visible.

Fig. 2. Measured current—voltage characteristics for two devices. (a) shows the behaviour of a 10 μm wide strip of graphene in device 2, showing evidence of Joule heating (non-linearity), whereas (b) shows the behaviour under application of currents large enough to induce failure. Local mini-failures occur just before total failure. (c) The behaviour of a section of device 1, again before failure – here the lower resistance and reduced Joule heating can be seen; (d) Failure of the section occurs cleanly as a single event; (e) stable tunnelling is observed across the resulting nanogap.

Fig. 3. AFM images of the devices. (a) Topography and (b) phase images of device 1 (image size = 45 μm); (c) topography and (d) phase images of a section of device 2 where the folds are visible as a network of bright lines. The failure region is indicated by the arrow (image size = 18 μm).

Fig. 4. Calculated current-voltage and thermal characteristics of a device. (a) Calculated current-voltage behaviour for device 2, corresponding to the data in Fig. 2(a), fitted using the parameters in Table 1; (b) Calculated Temperature distribution within the device; (c) variation of temperature at the centre of the device with current; (d) AFM image of the part-failed device 1, showing where tears have appeared in the graphene.

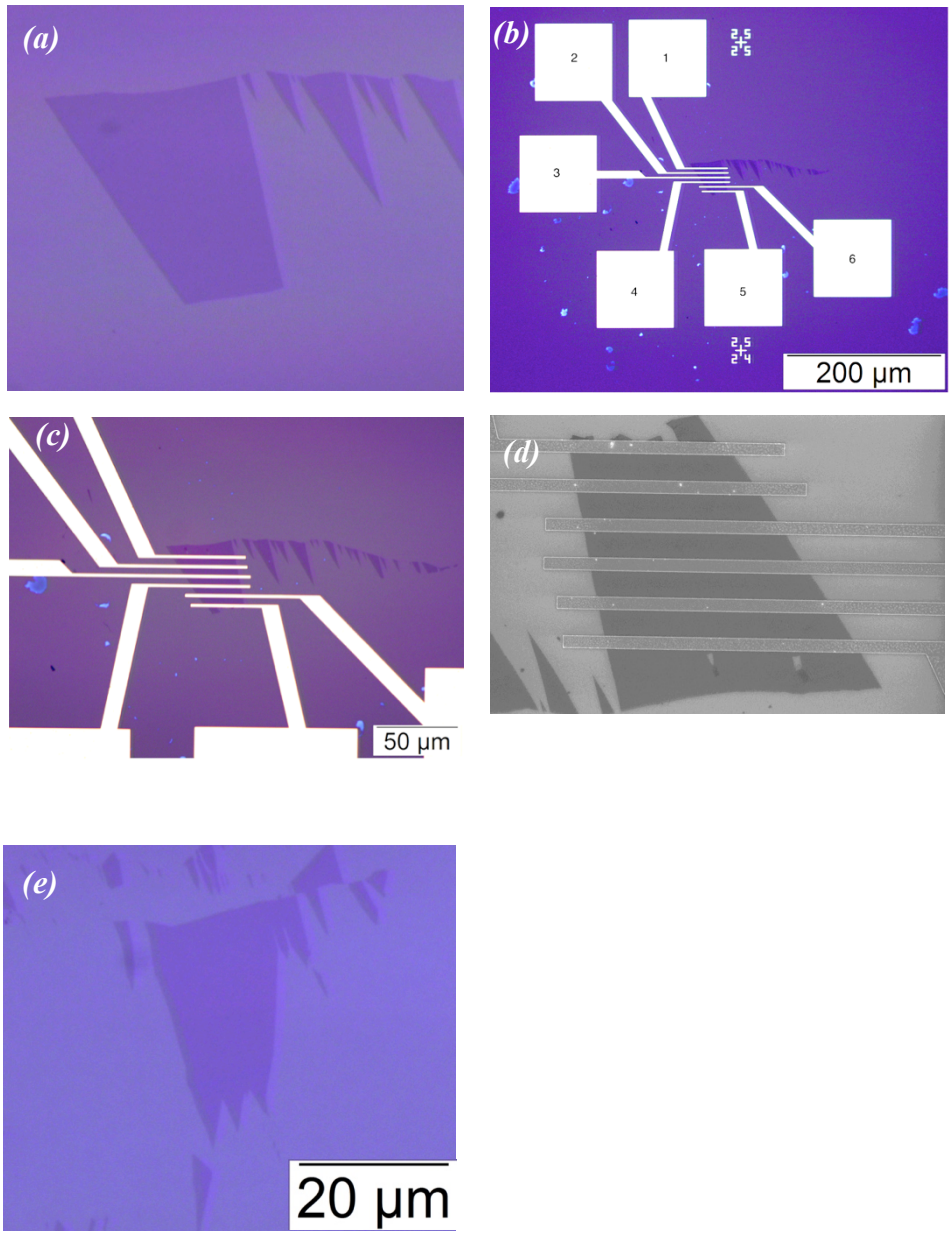

Fig. 1

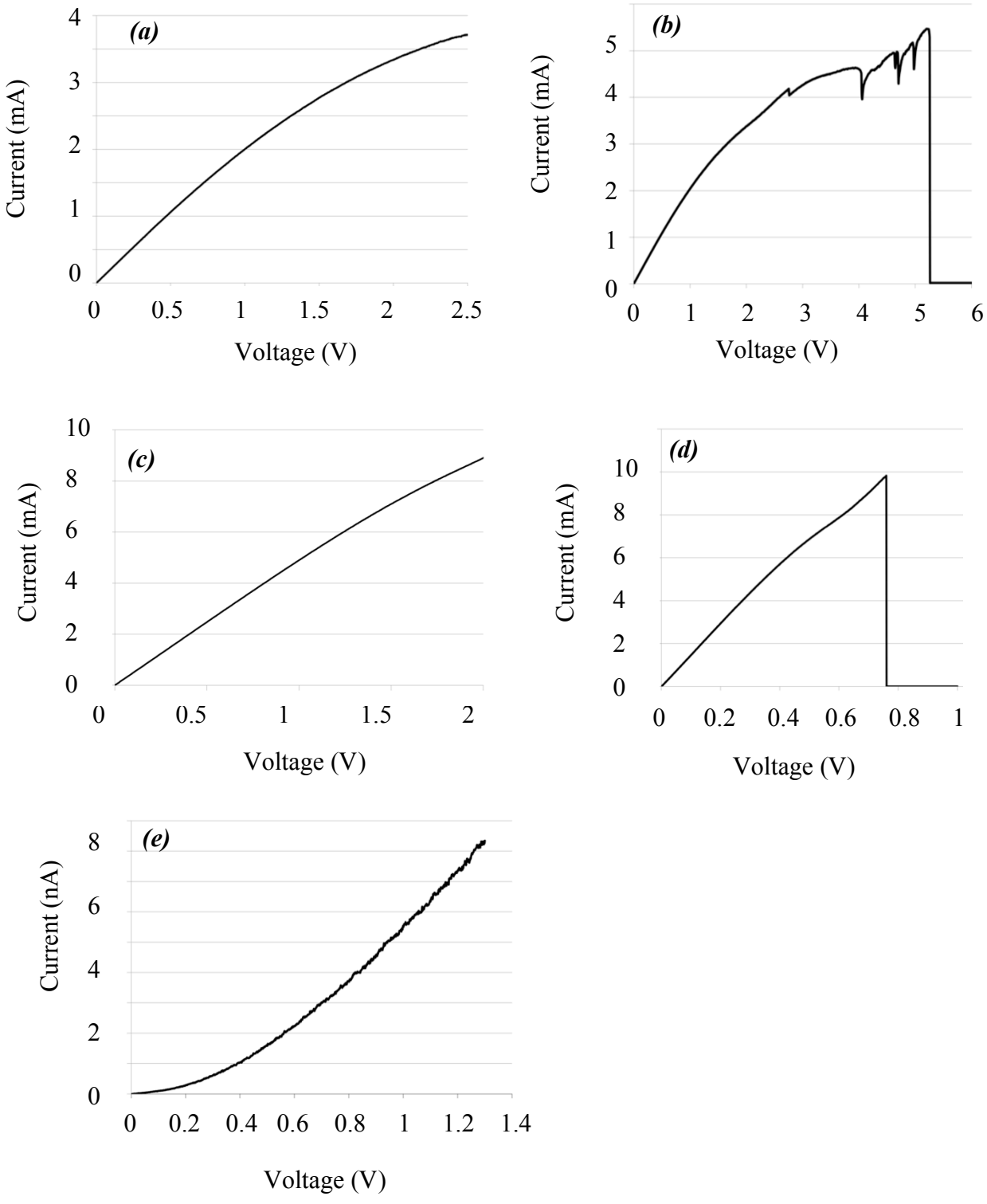
(a)
Current (mA)
Voltage (V)
(b)
Current (mA)
Voltage (V)
(c)
Current (mA)
Voltage (V)
(d)
Current (mA)
Voltage (V)
(e)
Current (nA)
Voltage (V)

Fig. 2

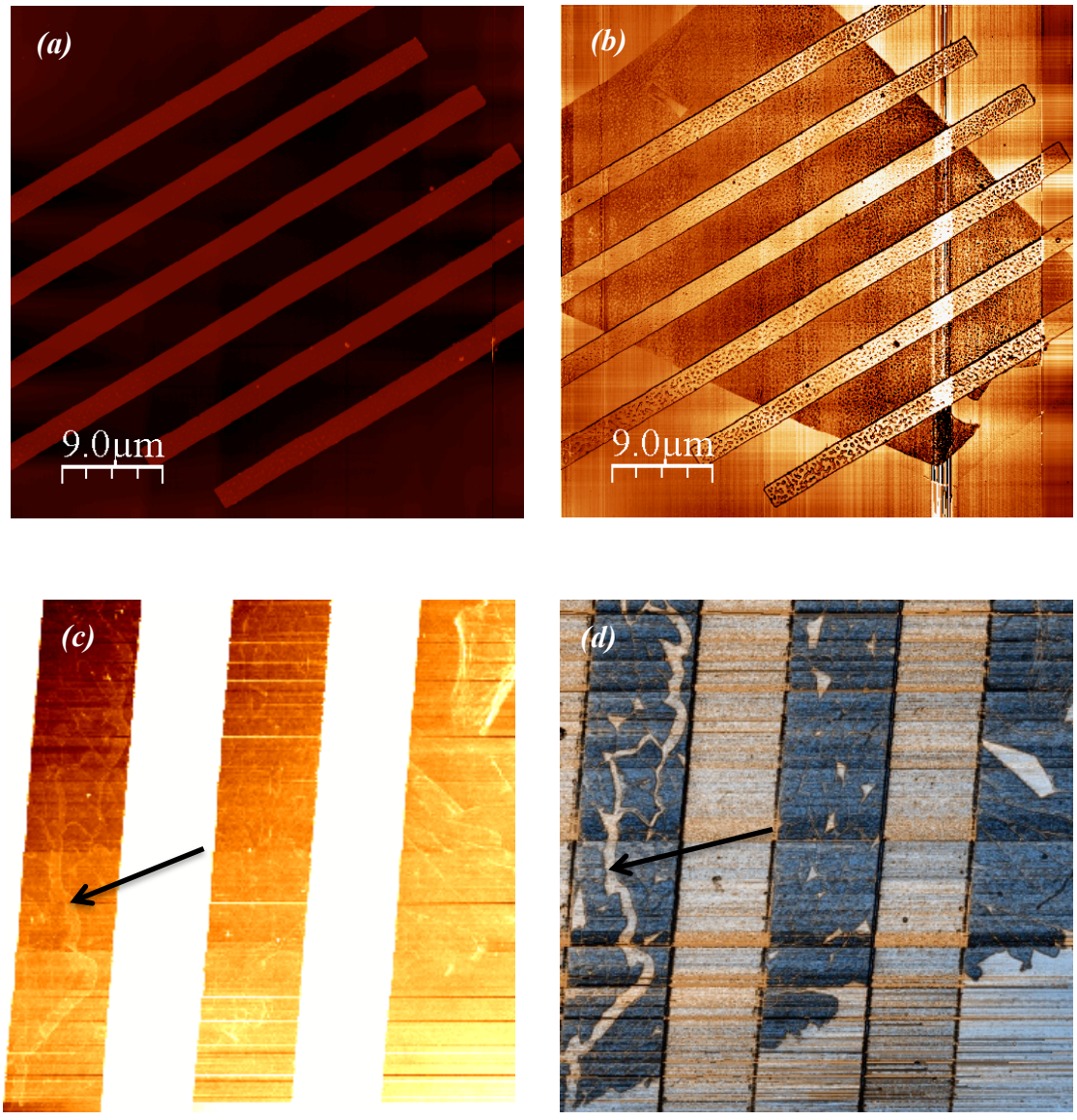

Fig. 3

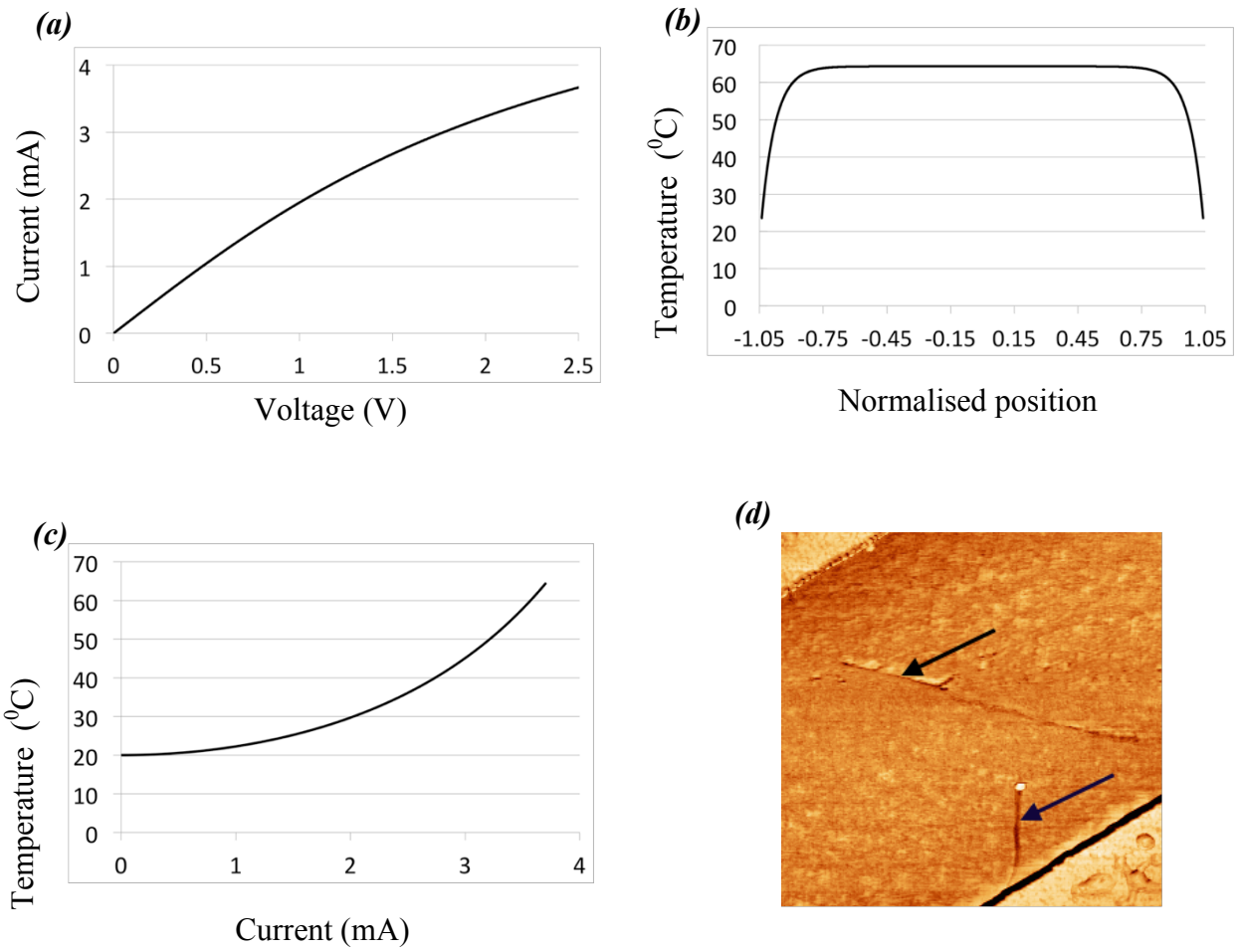
(a)
Current (mA)
0
1
2
3
4
0
0.5
1
1.5
2
2.5
Voltage (V)
(b)
Temperature (⁰C)
0
10
20
30
40
50
60
70
-1.05
-0.75
-0.45
-0.15
0.15
0.45
0.75
1.05
Normalised position
(c)
Temperature (⁰C)
0
10
20
30
40
50
60
70
0
1
2
3
4
Current (mA)
(d)

Fig. 4